Table 1: Processor statistics obtained from instruciton set simulation (ISS)

Apps	Cyc_{arith}	Cyc_{ld}	Cyc_{st}	Cyc_{jump}	Cyc_{br_taken}	$Cyc_{br\_untaken}$	Num_{imiss}	Num_{dmiss}	$Num_{uncache}$	$Num_{intlock}$
add4	230708	220040	110008	90066	30417	7	38	87	810	140015
bubsort	61979	80865	22807	23838	23709	7528	49	48	810	65135
byteswap	100709	150042	80010	60066	15417	5007	40	40	810	85016
rand_gene	530202	846352	351658	168624	138072	15483	133	163	810	571879
Alphablend	49709	36039	13008	9066	3417	7	45	88	810	27014
RGB_CMYK	31709	29039	15006	12654	5829	1203	43	86	810	19159

In this table, each row represents the statistic data obtained from instruction set simulation for each training program. They are in the sequence of: number of cycles for arithmetic instruction, # of cycles for load, # of cycles for store, # of cycles for jump, # of cycles for branch taken, # of cycles for branch untaken, # of instruction cache miss, # of data cache miss, # of uncached instruciton cache miss, # of processor interlock.